In the Claims:

1. (Currently Amended) A vertical field effect transistor comprising:

a microelectronic substrate including a trench, the trench defining a sidewall;

a conformal monocrystalline silicon layer on the sidewall of the trench, the conformal monocrystalline silicon layer on the sidewall of the trench including a drain region adjacent the substrate, a source region remote from the substrate and a channel region between the source and drain regions;

a plug comprising insulating material in the trench that includes the conformal monocrystalline silicon layer on the sidewall thereof;

a gate insulating layer adjacent the channel; and

a gate electrode on the gate insulating layer opposite the channel.

2. (Original) A field effect transistor according to Claim 1 wherein the conformal monocrystalline silicon layer on the sidewall of the trench is a continuous conformal monocrystalline silicon layer on the sidewall of the trench.

3. (Original) A field effect transistor according to Claim 1 wherein the conformal monocrystalline silicon layer on the sidewall of the trench comprises spaced apart conformal portions of the conformal monocrystalline silicon layer on the sidewall of the trench.

4. (Original) A field effect transistor according to Claim 1 further comprising:

a first layer on the substrate; and

a second layer on the first layer opposite the substrate;

wherein the trench extends in the first layer and the second layer; and

wherein the gate insulating layer and the gate electrode are between the first and second layers.

5. (Original) A field effect transistor according to Claim 4 wherein the first and second layers comprise phosphosilicate glass and/or borosilicate glass.

6. (Currently Amended) A field effect ~~transistors~~ transistor according to Claim 1 wherein the plug comprises high dielectric constant insulating material.

7. (Original) A field effect transistor according to Claim 1 further comprising a silicon layer between the microelectronic substrate and the drain region.